REMARKS

Claims 1 - 57 are pending in the application and are presented for reconsideration. The remaining independent claims are 1, 17, 19, and 46.

By the foregoing amendments, claims 1, 17, 19, and 46 are sought to be amended. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended merely to clarify the claims and expedite the prosecution of the application, not to overcome any cited references. In making these amendments, Applicants do not concede that the subject matter of such claims was in fact disclosed or taught by the cited art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections, and withdraw them.

Objection to the claims

In the second paragraph, the Office Action objects to claim 1 due to an informality. Accordingly, this portion of the claim has been amended to read "by causing thread-switching ~~between~~ from execution." Applicants thank the Examiner for identifying this issue and respectfully request that the Examiner reconsider and withdraw this objection.

Rejections under 35 U.S.C. §103

In the fourth paragraph, the Office Action rejects claims 1, 29-33, 42-43, and 45 under 35 USC § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,076,157 ("Borkenhagen") in view of U.S. Patent No. 6,374,286 ("Gee"). This rejection is respectfully traversed.

Claim 1 recites:

> A computer based system for switching between program contexts comprising:
>
> a processor capable of having a first program thread and a second program thread in an execution pipeline having thread selection hardware;
>
> a first set of data storage devices capable of storing a first thread state of said processor;
>
> a second set of data storage devices capable of storing a second thread state of said processor; and
>
> a hardware thread scheduler for identifying which of said program threads said processor executes and configurable to allocate available processing time of the processor among at least the first and second program threads by causing thread-switching from execution of the first program thread directly to execution of the second program thread at a fixed time according to a predetermined fixed schedule and without using interrupts by accessing one or more registers included in the first set or the second set of data storage devices based on a context number associated with an instruction included in a program thread identified for execution by the predetermined fixed schedule, said schedule specifying that the first thread should be allocated processing time every first number of cycles and that the second thread should be allocated processing time every second number of cycles, wherein said first number of cycles is not equal to said second number of cycles.

The hardware thread scheduler recited in claim 1 is configurable so the processor switches from the execution of one thread directly to the execution of another thread according to a predetermined fixed schedule, not by invoking an interrupt. This beneficially provides a predictable execution time for threads, allowing each thread to be executed for a predetermined number of instruction cycles specified by the predetermined fixed schedule. Additionally, by switching directly from the first thread to the second thread (in contrast to using an interrupt), the

hardware thread scheduler reduces the overhead associated with switching between threads, allowing more time for execution of instructions from different threads. *See* spec., page 25, lines 8-13; page 27, line 4 to page 28, line 9. As disclosed on page 25 and 26 of the spec, "A counter 904 is used to point to the time slices in the registers in the HRT selector 802." and "The counter 904 is used in conjunction with the bank selector 902 to identify the thread that will be fetched by the shadow SRAM in the following cycle." This indicates that that the next scheduled HRT thread is loaded without the use of interrupts. In addition, page 26 of the spec states "More signals could be used to control more threads. One signal is used to indicate that no HRT thread is to be fetched." Since the claimed invention has a signal which indicates that no HRT thread is to be fetched in a given cycle, it is evident that an attempt to fetch an HRT thread is made during each cycle regardless of any interrupt.

The claimed invention has signals which are read in order to determine which HRT thread, if any, should be loaded. In contrast, Gee indicates that an interrupt from a timer sets off the piano roll. For example, Gee states "The piano roll is driven by a periodic interrupt called a "tick" which is usually generated by a hardware timer." (Gee, col. 20, ll. 47-49) and "At time 1401, a partition interrupt, which is a non-maskable interrupt, occurs. The interrupt causes the JEM microcode in the processor to vector to an NMI interrupt handler." (Gee, col. 25, ll. 30-33). Gee's use of an interrupt handler causes its method to be less efficient and slower than the claimed invention. Therefore, the addition of Gee would not overcome the shortcomings of Borkenhagen with respect to the claimed invention.

In the 14th paragraph, the Office Action rejects claims 2-4, 13, 16-17, 19-24 and 56-57 under 35 USC § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,542,991 ("Joy") in view of "Using Horizontal Prefetching to Circumvent the Jump Problem" ("McCrackin"). This rejection is respectfully traversed.

The independent claims 17 and 19 have been amended to include language similar to claim 1 regarding a lack of interrupts. The examiner does not contend that Joy or McCrackin overcome the deficiencies of Borkenhagen and Gee. Further, McCrackin does not disclose thread switching according to a predetermined fixed schedule and could not operate in the same manner as the claimed invention.

In the 68th paragraph, the Office Action rejects claims 46 and 47 under 35 USC § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,076,157 ("Borkenhagen") in view of U.S. Patent No. 6,374,286 ("Gee") and further in view of "Using Horizontal Prefetching to Circumvent the Jump Problem" ("McCrackin"). This rejection is respectfully traversed.

Claim 46 has been amended to contain language similar to claim 1. Therefore, the arguments above regarding the deficiencies of Gee and McCrackin apply to claim 46 as well.

The office action takes official notice that "virtually all caches are implemented with static RAM (SRAM) and that SRAM and its advantages are well known and accepted in the art." The office action also takes took official notice that "flash-based main memories and their

advantages are well known and accepted in the art." Official notice unsupported by documentary evidence may be taken only where the officially noticed facts are capable of "instant and unquestionable demonstration." But the MPEP cautions that "assertions of technical facts in the areas of . . . specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art." MPEP § 2144.03; *see also In re Ahlert*, 424 F.2d 1088, 1091, 165 U.S.P.Q. (BNA) 418, 420-21 (CCPA 1970). In this case, the facts officially noticed by the examiner were in the area of "specific knowledge of the prior art," as opposed to facts that are "capable of instant and unquestionable demonstration"; therefore, the official notice was improper.

On this basis, Applicants challenge the office action's assertions of officially noticed facts and request that the USPTO produce authority for this assertion, or in the alternative, withdraw all rejections that are based on the facts officially noticed. Applicants do not admit any of the officially noticed facts and reserve the right to argue against the examiner's assertions at a later time, if necessary.

Based on the above amendments and the remarks, Applicants respectfully submit that for at least these reasons claims 1, 17, 19, and 46 are patentably distinguishable over the cited references. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

As claims 2-16, 18, 20-45, and 47-57 are dependent on claims 1, 17, 19, and 46, all arguments advanced above with respect to claims 1, 17, 19, and 46 are hereby incorporated so as to apply to claims 2-16, 18, 20-45, and 47-57.

In summary, the Office Action has failed to point out any art teaching which anticipates or renders obvious the explicit recitation in the language of claim 1 "allocate available processing time of the processor among at least the first and second program threads by causing thread-switching from execution of the first program thread directly to execution of the second program thread at a fixed time according to a predetermined fixed schedule and without using interrupts." Therefore, it is respectfully submitted that the rejections are improper and should be withdrawn.

Conclusion

Applicants believe that all of the stated grounds of objection and rejection set forth in the Office Action have been properly accommodated or addressed. Applicants, therefore, respectfully request that the Examiner reconsider all presently outstanding objections and rejections and withdraw them. The Examiner is invited to telephone the undersigned representative if it is felt that an interview might be useful for any reason.

Respectfully submitted

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By: /John T. McNelis/

John T. McNelis
Attorney for Applicants
Reg. No. 37,186
FENWICK & WEST LLP
Silicon Valley Center
801 California Street
Mountain View, CA 94041
(650) 335-7133
jmcnelis@fenwick.com